

SHENZHEN TIBTRONIX TECHNOLOGY CO., LTD.

TPPLFH40D4

**400Gb/s QSFP-DD ER4 40km Transceiver Hot Pluggable, Dual LC Connectors, Single mode
4x100Gb/s EML+PIN with SOA**

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Features:

- ✧ 4 Narrow LANWDM laser and PIN receiver with SOA;
- ✧ QSFP-DD MSA package with duplex LC connector;
- ✧ Compliant to IEEE 802.3bs QSFP-DD Specification
- ✧ Compliant with QSFP-DD CMIS standard
- ✧ 8x53.125Gb/s with PAM4 electrical interface (400GAUI-8)
- ✧ Up to 40km transmission on single mode fiber (SMF)
- ✧ Maximum power consumption 13W
- ✧ Single +3.3V power supply operating
- ✧ Temperature range 0°C to 70°C
- ✧ RoHS Compliant Part

Applications:

- ✧ 400G BASE-ER4 Ethernet Links
- ✧ Data center Interconnect
- ✧ Infiniband Interconnect
- ✧ Enterprise Networking

Description:

The TPPLFH40D4 is a 400Gb/s QSFP-DD optical module designed for 40km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of narrow LAN WDM optical signals and multiplexes them into a single channel for 400Gb/s optical transmission.

on the receiver side, an optical de-multiplexer is coupled to a 4 channel PIN with SOA array and converts them to 8 channels of 50Gb/s (PAM4) electrical output data.

The central wavelengths of the 4 narrow LAN WDM channels are 1304nm, 1306nm, 1309nm and 1311nm.

● Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	T_S	-40		+85	°C
Supply Voltage	$V_{CC,T,R}$	-0.5		4	V
Relative Humidity	RH	0		85	%

● Recommended Operating Environment:

Parameter	Symbol	Min.	Typical	Max.	Unit
Case operating Temperature	T_C	0		+70	°C
Supply Voltage	$V_{CCT,R}$	+3.13	3.3	+3.47	V
Supply Current	I_{CC}			3900	mA
Power Dissipation	PD			13	W

● Electrical Characteristics ($T_{OP} = 0$ to 70 °C, $V_{CC} = 3.13$ to 3.47 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data Rate per Channel		-	26.5625		Gbps	
Differential Input Return Loss		9.5-0.37f			dB	
Differential termination mismatch				10	%	
Transmitter						
Single Ended Output Voltage Tolerance		0.3		4	V	
Transmit Input Diff Voltage	V_I	900			mV	1
Differential Input Return Loss (min)		IEE 8002.3-2015 Equation(83e-5)			dB	
Differential to Common Mode Input Return Loss (min)		IEE 8002.3-2015 Equation(83e-6)			dB	
Module Stressed Input Test		Per Section 120E.3.4.1,IEEE802.3bs				2
Single-ended Voltage Tolerance Range(min)		-0.4 to 3.3			V	
DC Common Mode input Voltage		-350		2850	mV	3
Receiver						
Single Ended Output Voltage Tolerance		0.3		4	V	
Rx Output Diff Voltage	V_O			900	mV	1
AC Common Mode Output Voltage,RMS				17.5	mV	
Differential Output Return Loss (min)		IEEE 802.3-2015 Equation(83E-2)				
Common to Differential Mode Conversion Return Loss (min)		IEEE 802.3-2015 Equation(83E-3)				
Near-end ESMW(Eye symmetry mask width)			0.265		UI	
Far-end ESMW(Eye symmetry mask width)			0.2		UI	

Near-end Eye height,differential		70			mV	
Far-end Eye height,differential		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Rx Output Rise and Fall Voltage	Tr/Tf	9.5			ps	1
Common Mode Output Voltage(Vcm)		-350		2850	mV	

Note:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

● Optical Parameters(TOP = 0 to 70 °C, VCC = 3.0 to 3.6 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Modulation Format	PAM4					
Lane Wavelength Range	Lane 0	1304.06	1304.58	1305.10	nm	
	Lane 1	1306.33	1306.85	1307.38	nm	
	Lane 2	1308.61	1309.14	1309.66	nm	
	Lane 3	1310.90	1311.43	1311.96	nm	
Average Optical Power each lane	Po	1.5		7.1	dBm	1
Total Average launch power				13.1	dBm	
Optical Modulation Amplitude (OMA), each lane	Po_OMA	4.5		7.9	dBm	2
Difference in launch power between any two lanes				4	dB	
Transmitter and Dispersion Eye Closure for PAM4,each Lane	TDECQ			3.9	dB	
TDECQ-10*log ₁₀ (Ceq),each Lane				3.9	dB	3
Extinction Ratio	ER	6			dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Relative Intensity Noise	Rin			-136	dB/HZ	
Side-mode Suppression Ratio	SMSR	30	-	-	dB	
Optical Return Loss Tolerance		-	-	15.6	dB	
Transmitter Reflectance				-26	dB	
Receiver						
Modulation Format	PAM4					
	Lane 0	1304.06	1304.58	1305.10	nm	
	Lane 1	1306.33	1306.85	1307.38	nm	

Lane Wavelength Range	Lane 2	1308.61	1309.14	1309.66	nm	
	Lane 3	1310.90	1311.43	1311.96	nm	
Damage Threshold,each Lane	THd	-2.4			dBm	4
Average Receive Power, each Lane	R	-16.5		-3.4	dBm	5
Receiver Sensitivity (OMA) per Lane	Rxsens			-14	dBm	6
RSSI Accuracy		-2.5		2.5	dB	
Receiver Reflectance	Rrx			-26	dB	
LOS De-Assert	LOS _D			-18	dBm	
LOS Assert	LOS _A	-28			dBm	
LOS Hysteresis	LOS _H	1.5			dB	

Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3dB for an extinction ratio of < 4.5dB, the OMA_{outer} (min) must exceed the minimum value specified here.
3. Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
6. Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.9 dB. It should meet Equation (1).

$$RS = \max(-6.6, SECQ - 8.0) \text{ dBm (1)}$$
Where:
RS is the receiver sensitivity, and
SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.
7. Measured with conformance test signal at TP3 for the BER equal to 2.4×10^{-4} .

● Pin Assignment

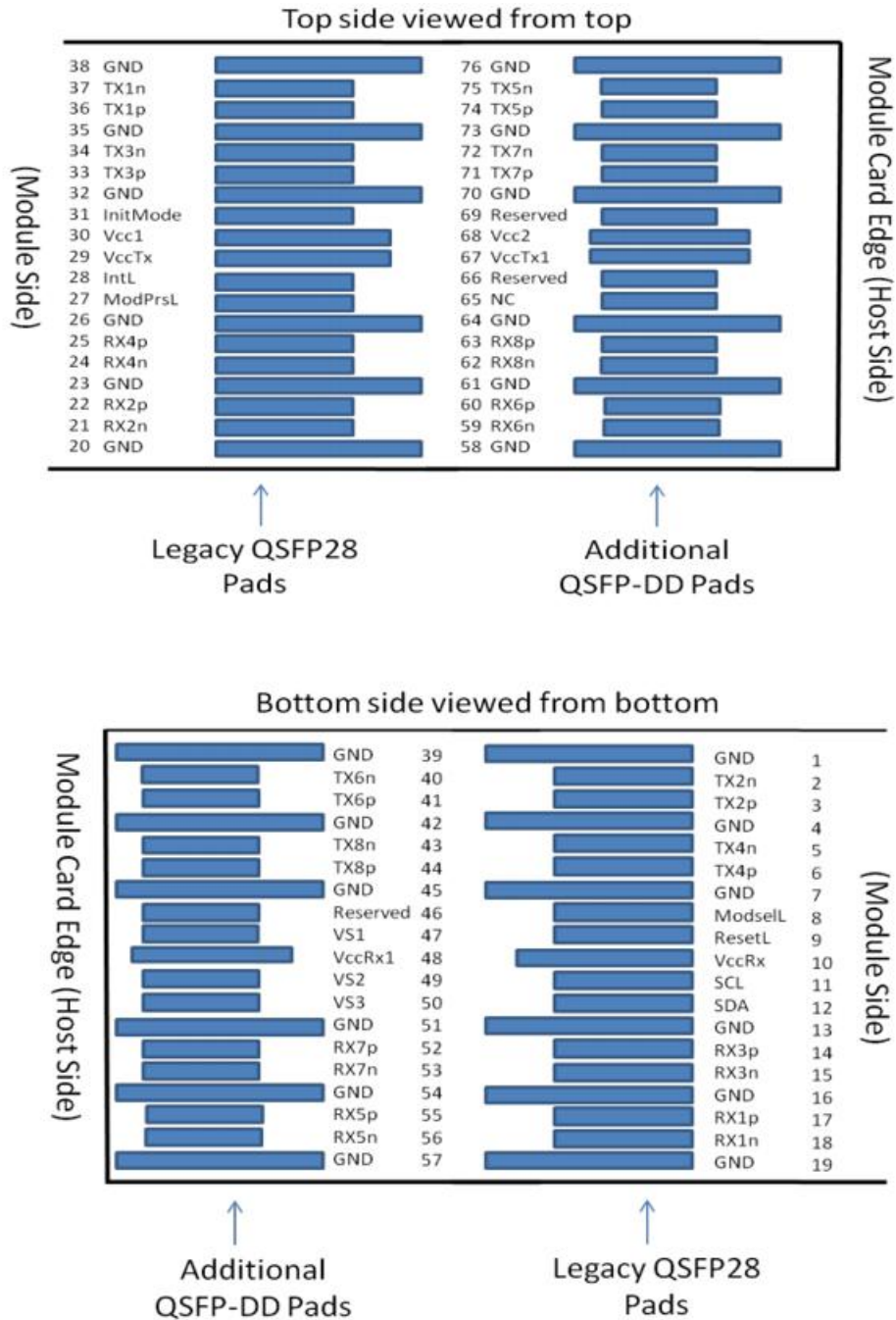


Diagram of Host Board Connector Block Pin Numbers and Name

● Pin Description

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	

6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTTL-I	ModSelL	Module Select	
9	LVTTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	TWI serial interface clock	
12	LVC MOS-I/O	SDA	TWI serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTTL-O	ModPrsL	Module Present	
28	LVTTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	
29		VccTx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTTL-I	LPMODE/TxDis	Low Power mode/optional TX Disable	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	

45		GND	Ground	1
46	LVC MOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	5
47	LVC MOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	5
48		VccRx1	3.3V Power Supply	2
49	LVC MOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	5
50	LVC MOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	5
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69	LVC MOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

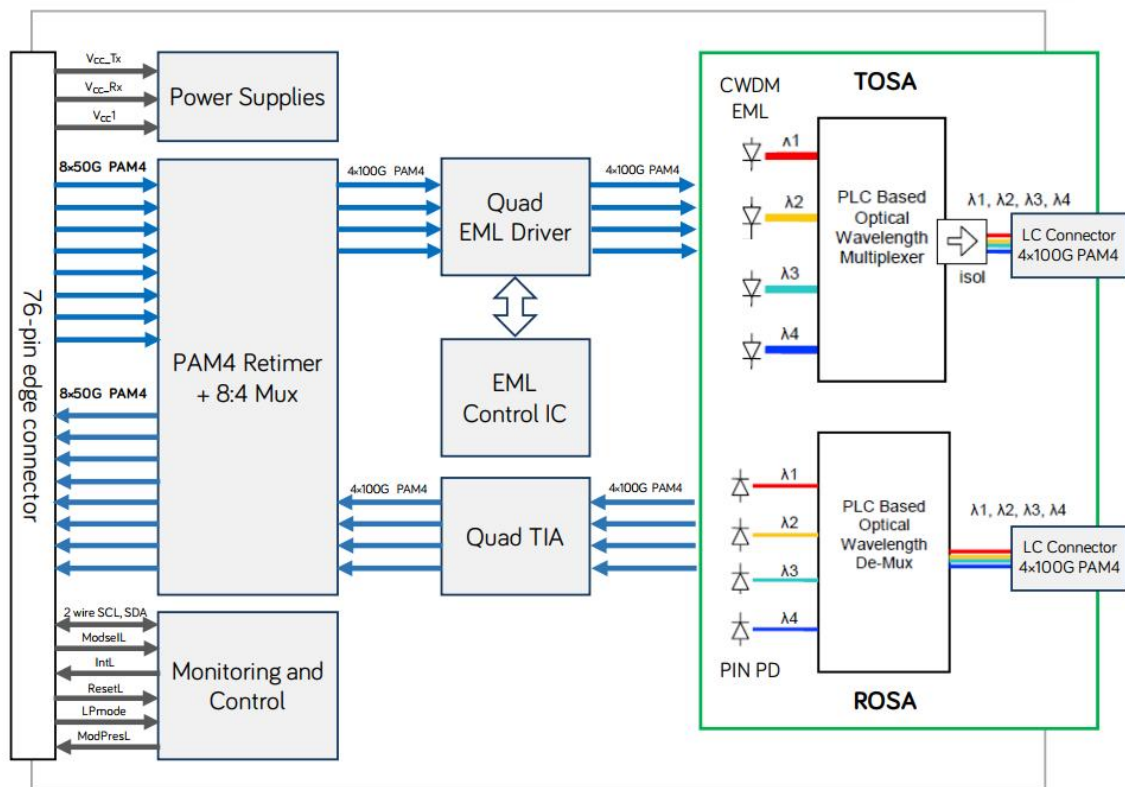
Notes:

1. GND is the symbol for single and supply(power) common for QSFP modules, All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx

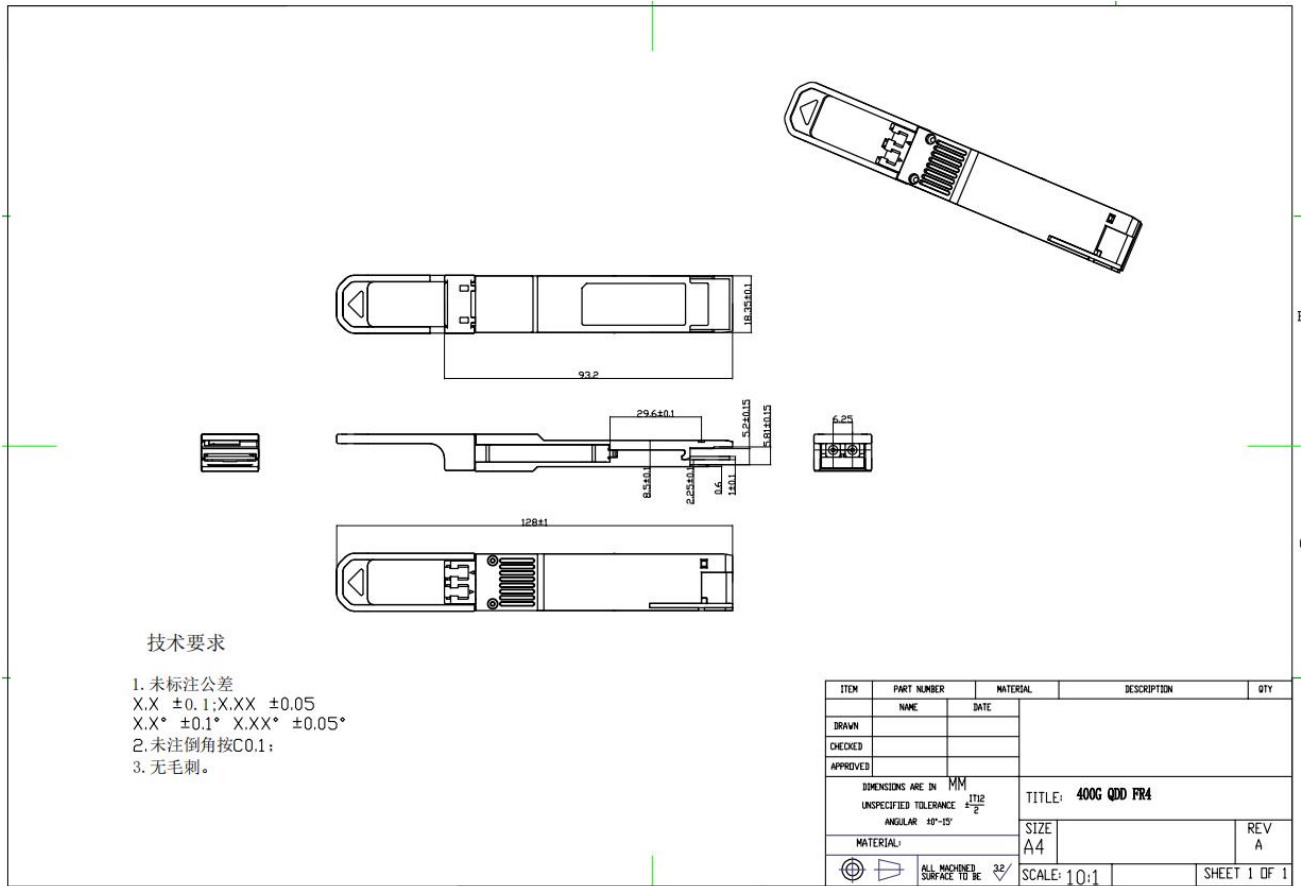
may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 2k mA.

3. Reserved pad recommended to be terminated with 10 k Ω to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10 k Ω to ground on the host.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (See Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP- DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.
5. Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 k Ω . For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 k Ω .

● Module Block Diagram



● Mechanical Dimensions



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