

TIBTRONIX TECHNOLOGY CO., LTD.



# T8PLHGA0D

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100Gb/s 100km QSFP28 Transceiver Hot Pluggable, Duplex LC Connector, EML+PIN with SOA Single mode DDM

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## Features:

- ✧ 4 lanes MUX/DEMUX design
- ✧ Support 100GBASE-ZR4 for line rate of 103.125Gbps and OTU4 for line rate of 111.81Gbps LAN WDM EML laser and PIN receiver with SOA
- ✧ Aggregate bandwidth of > 100Gbps
- ✧ Duplex LC connectors
- ✧ Compliant with IEEE 802.3-2012 Clause 88 standard IEEE 802.3bm CAUI-4 chip to module electrical standard ITU-T G.959.1-2012-02 standard
- ✧ Single +3.3V power supply operating
- ✧ Built-in digital diagnostic functions
- ✧ Temperature range 0°C to 70°C
- ✧ RoHS Compliant Part
- ✧ Support FEC(Forward Error Correction)

## Applications:

- ✧ 100GBASE-ZR4

## Description:

- ✧ TIBTRONIX's T8PLHGA0D is designed with metal protection for 100km optical communication applications. This module contains 4-lane optical transmitter, 4-lane optical receiver and module management block including 2 wire serial inter-face. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector. A block diagram is shown in Figure 1.

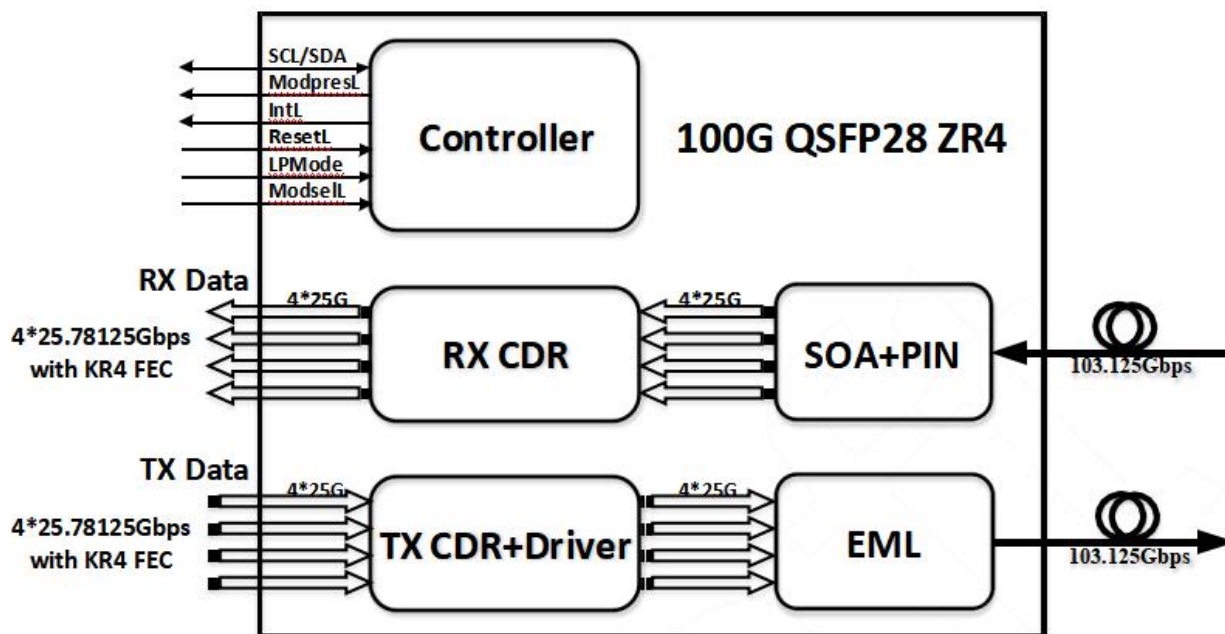


Figure 1. Transceiver Block Diagram

### ● Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	$T_S$	-40		+85	°C
Supply Voltage	$V_{CC,T,R}$	-0.5		4	V
Relative Humidity	RH	0		85	%

### ● Recommended Operating Environment:

Parameter	Symbol	Min.	Typical	Max.	Unit
Case operating Temperature	$T_C$	0		+70	°C
Supply Voltage	$V_{CC,T,R}$	+3.13	3.3	+3.47	V
Supply Current	$I_{CC}$		1200	1800	mA
Power Dissipation	PD			6.5	W

## ● Electrical Characteristics ( $T_{OP} = 0$ to $70$ °C, $V_{CC} = 3.13$ to $3.47$ Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data Rate per Channel		-	25.78125		Gbps	
			27.9525			
Power Consumption		-	4	6.5	W	
Supply Current	I <sub>cc</sub>		1.2	1.8	A	
Control I/O Voltage-High	V <sub>IH</sub>	2.0		V <sub>cc</sub>	V	
Control I/O Voltage-Low	V <sub>IL</sub>	0		0.7	V	
Inter-Channel Skew	TSK			35	Ps	
RESETL Duration			10		Us	
RESETL De-assert time				100	ms	
Power On Time				100	ms	
<b>Transmitter</b>						
Single Ended Output Voltage Tolerance		0.3		V <sub>cc</sub>	V	1
Common mode Voltage Tolerance		15			mV	
Transmit Input Diff Voltage	V <sub>I</sub>	150		1200	mV	
Transmit Input Diff Impedance	Z <sub>IN</sub>	85	100	115		
Data Dependent Input Jitter	DDJ		0.3		UI	
<b>Receiver</b>						
Single Ended Output Voltage Tolerance		0.3		4	V	
Rx Output Diff Voltage	V <sub>o</sub>	370	600	950	mV	
Rx Output Rise and Fall Voltage	Tr/Tf			35	ps	1
Total Jitter	TJ		0.3		UI	

Note:

1. 20~80%

## ● Optical Parameters(TOP = 0 to 70 °C, VCC = 3.0 to 3.6 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
<b>Transmitter</b>						
Wavelength Assignment	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Side-mode Suppression Ratio	SMSR	30	-	-	dB	

Total Average Launch Power	PT	8	-	12.5	dBm	
Average Launch Power, each Lane		+4	-	7.5	dBm	
Difference in Launch Power between any two Lanes (OMA)		-	-	3	dB	
Extinction Ratio	ER	6	-	-	dB	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				1
Optical Return Loss Tolerance		-	-	20	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Relative Intensity Noise	Rin			-130	dB/HZ	
Optical return loss tolerance				20	dB	
Transmitter reflectance		-	-	12	dB	
<b>Receiver</b>						
Total Damage Threshold	THd			5.5	dBm	1
Receiver Sensitivity per Lane	R			-28	dBm	
Average Power at Receiver Input, each Lane	R	-28		0	dBm	1
LOS De-Assert	LOS <sub>D</sub>			-31	dBm	
LOS Assert	LOS <sub>A</sub>	-40			dBm	
LOS Hysteresis	LOS <sub>H</sub>	0.5			dB	

#### Note

1. Sensitivity is specified at BER@5E-5 with FEC

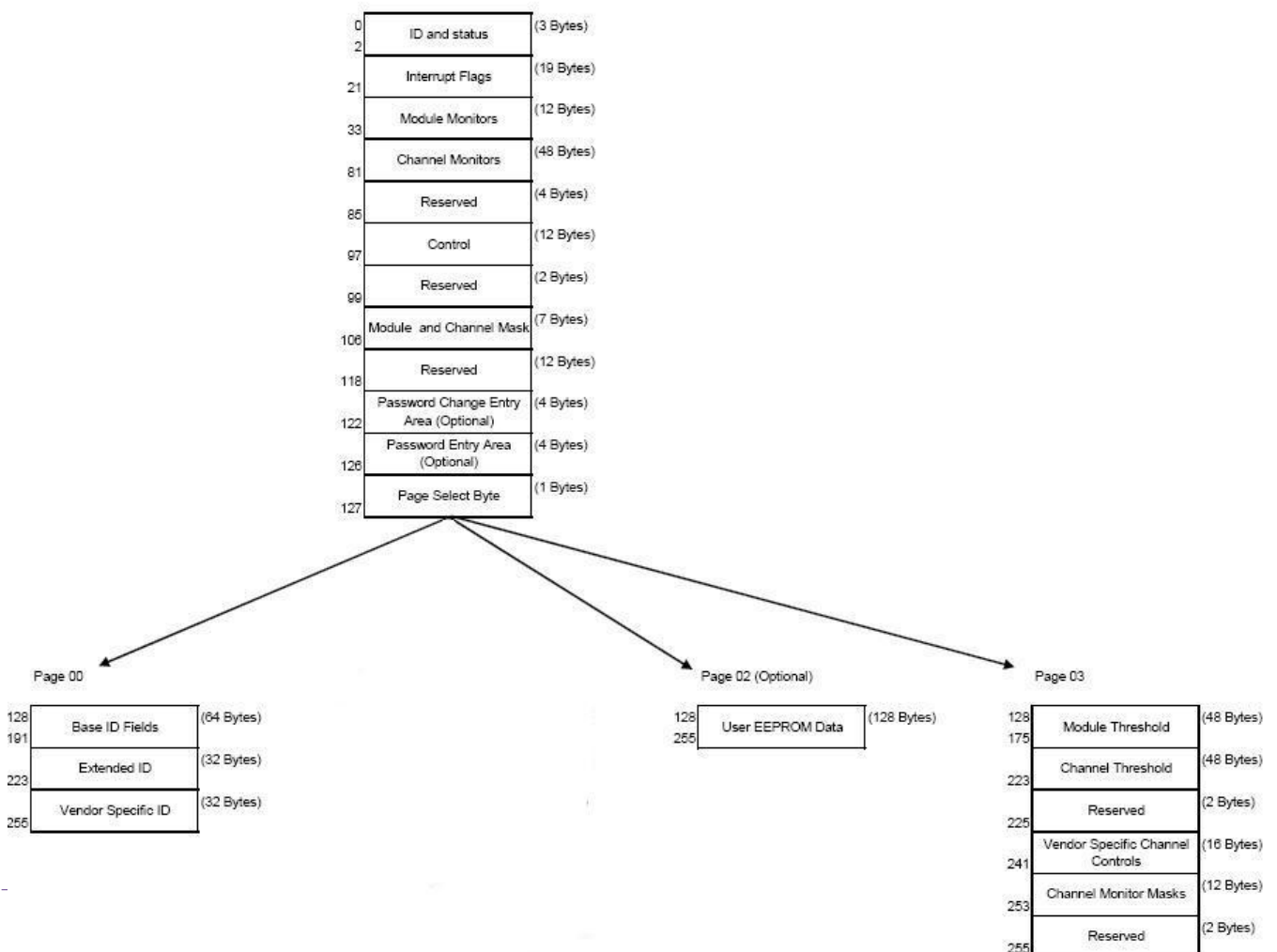
## ● Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on all QSFP28 ZR4. A 2-wire serial interface provides user to contact with module. The structure of the memory is shown in flowing. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

2-wire serial address, 1010000x (A0h)\*



Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mbits/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 $\mu$ m (1 Byte)	Link length supported for EBW 50/125 $\mu$ m fiber, units of 2 m
144	Length 50 $\mu$ m (1 Byte)	Link length supported for 50/125 $\mu$ m fiber, units of 1 m
145	Length 62.5 $\mu$ m (1 Byte)	Link length supported for 62.5/125 $\mu$ m fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand <sup>†</sup>
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and page00.page03 upper memory please see SFF-8436 document.

## ● Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on <sup>1</sup> , hot plug or rising edge of Reset until the module is fully functional <sup>2</sup>
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on <sup>1</sup> until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on <sup>1</sup> to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional <sup>2</sup>
LPMMode Assert Time	ton_LPMMode	100	μs	Time from assertion of LPMMode (Vin:LPMMode =Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	toff_IntL 500 μs Time from clear on read <sup>3</sup> operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set <sup>4</sup> until associated IntL assertion is inhibited
Mask De-assert Time	toff_mask	100	ms	Time from mask bit cleared <sup>4</sup> until associated IntL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_override or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set <sup>4</sup> until module power consumption enters lower Power Level

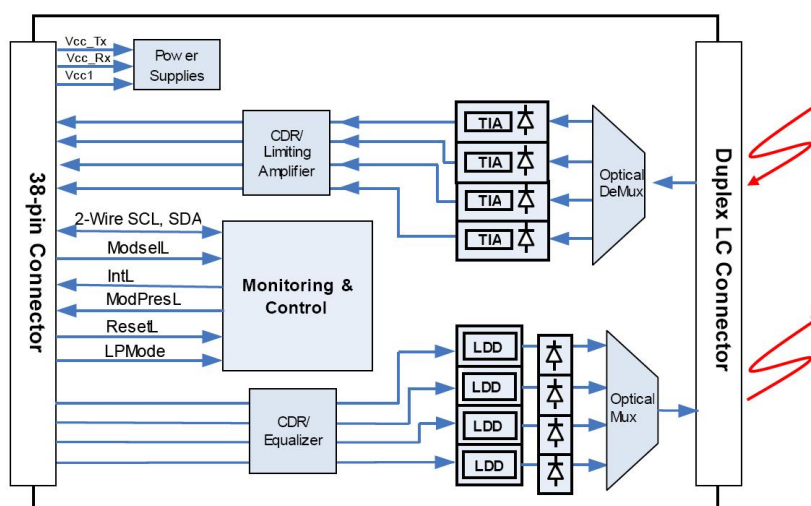


Power_override or Power-set De-assert Time	toff_Pdown	300	ms	Time from P_Down bit cleared <sup>4</sup> until the module is fully functional <sup>3</sup>
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**Note:**

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

● **Transceiver Block Diagram**



● **Pin Assignment**

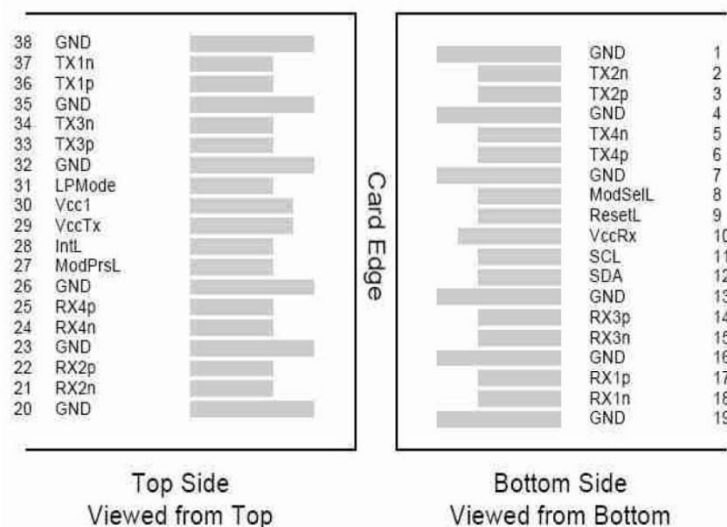


Diagram of Host Board Connector Block Pin Numbers and Name

## ● Pin Description

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMODE	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1

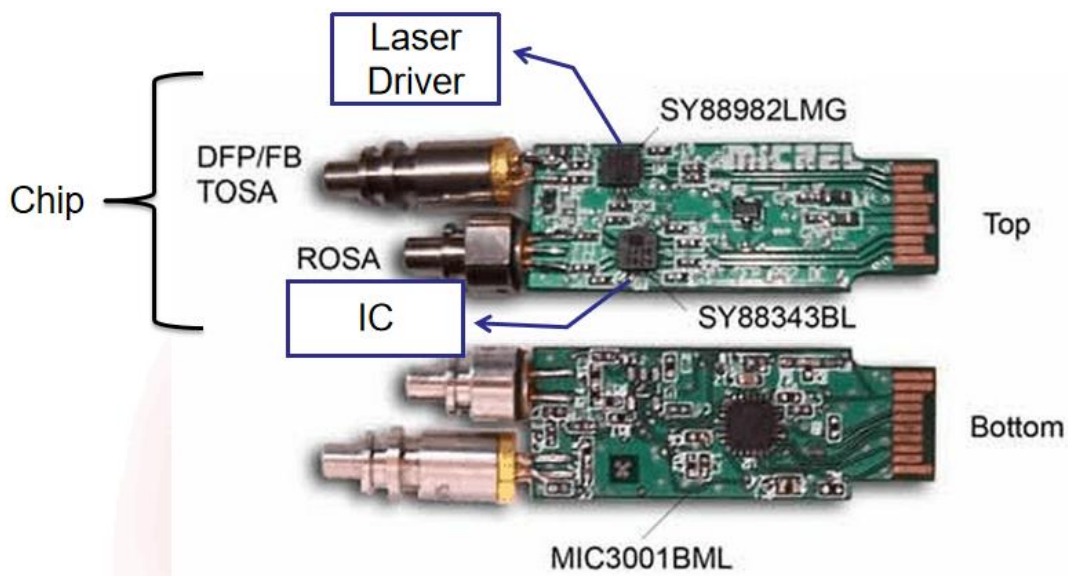
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

**Notes:**

1. GND is the symbol for single and supply(power) common for QSFP28 modules, All are common within the QSFP28 module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for maximum current of 500mA.

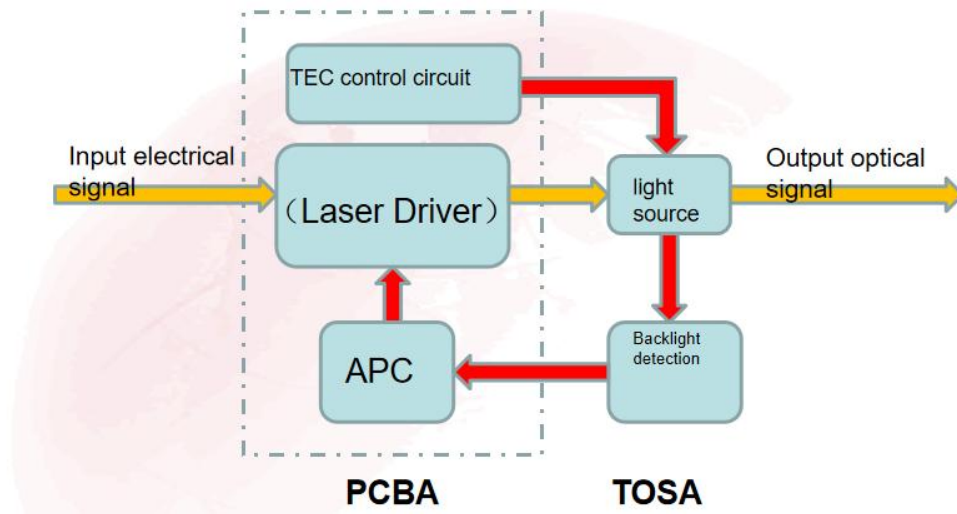
## ● More Basic Information

### Composition of the general model with main components

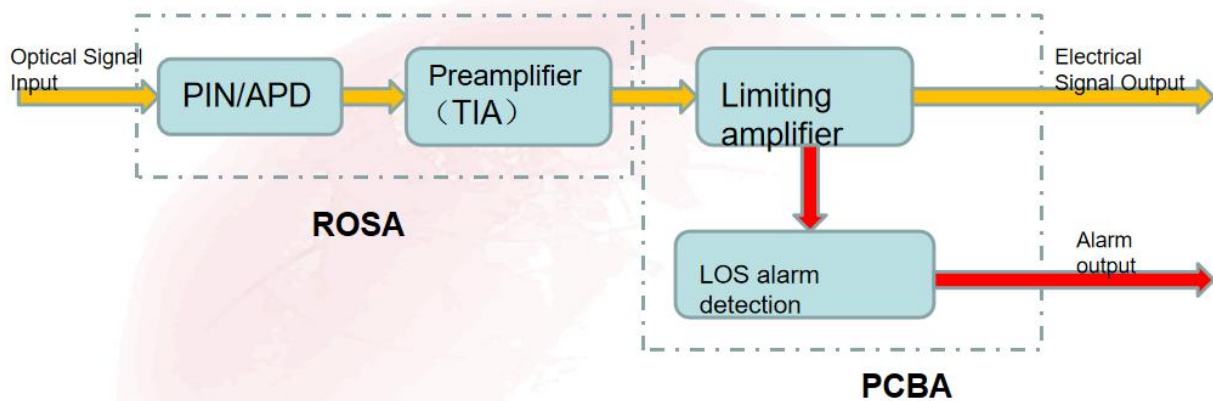


### Working Principle

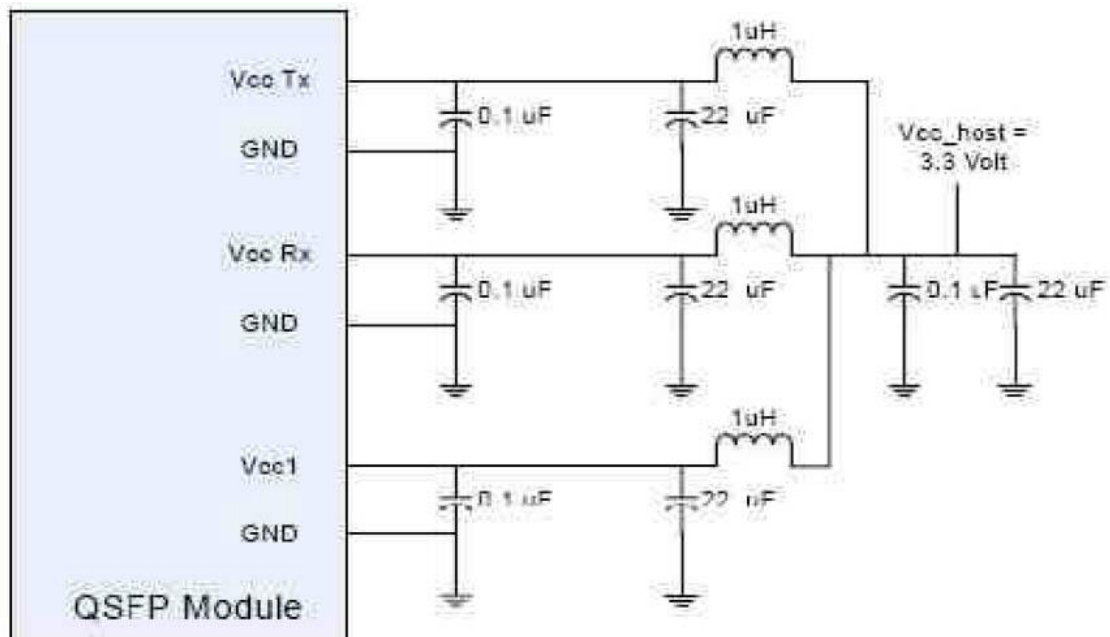
## ➤ Transmitting terminal working principle :



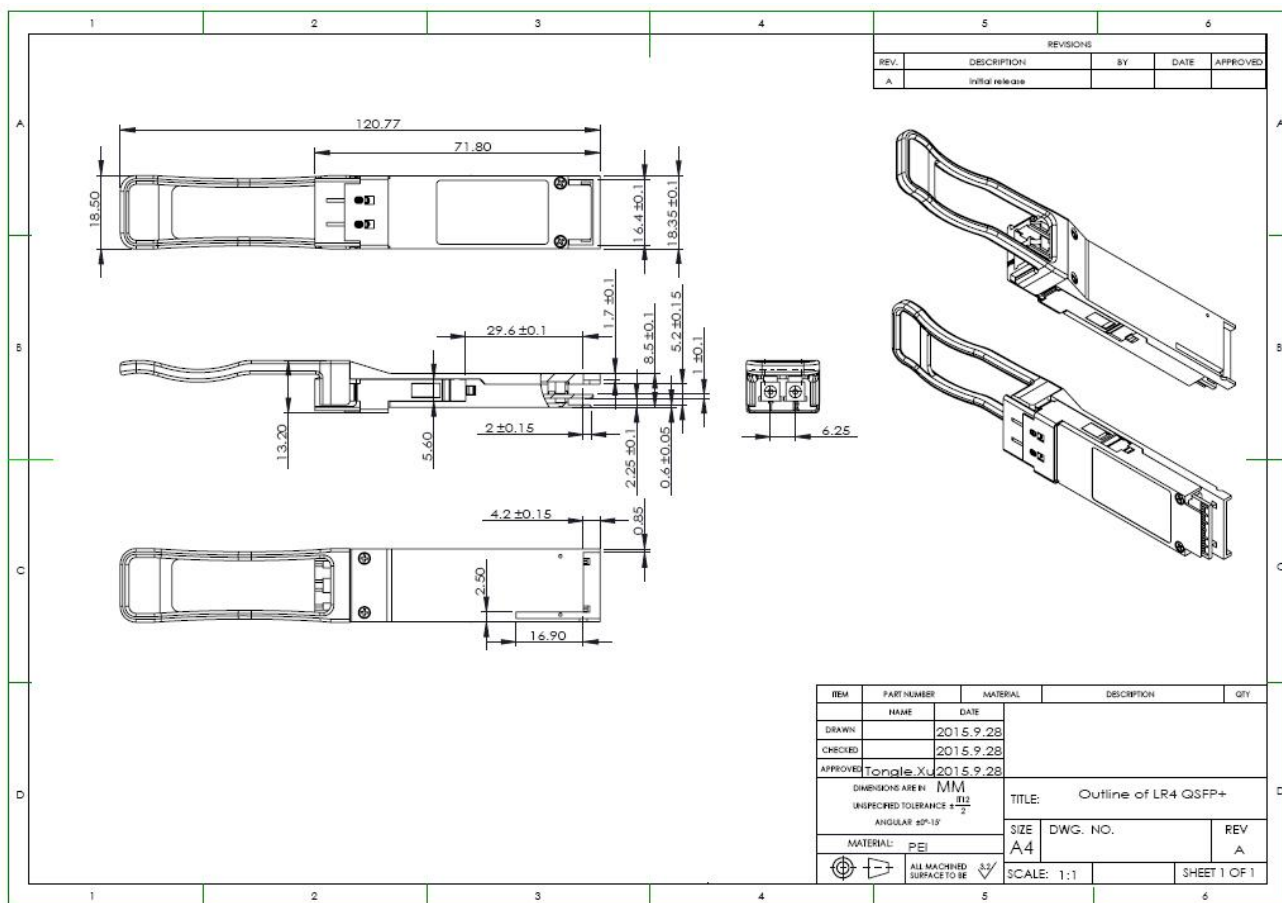
## ➤ Receiving terminal working principle:



- Recommended Circuit



### Mechanical Dimensions



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